OIPE IAP2
FEB 0 3 2006
PATENT & TRADEMARK OFFICE

Docket No.: Z&P-INFN10356

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

MAIL STOP: APPEAL BRIEF-PATENTS

By: _____ Date: January 30, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applic. No.	:	10/623,068 Confirmation No.: 2691
Inventor	:	Hans-Jörg Timme, et al.
Filed	:	July 18, 2003
Title	:	Filter Device and Method for Fabricating Filter Devices
TC/A.U.	:	2822
Examiner	:	Maria Guerrero
Customer No.	**:**	**24131**

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

S i r :

This is an appeal from the final rejection in the Office action dated September 20, 2005, finally rejecting claims 22-29 and 32-34.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $500.00 to cover the fee for filing the *Brief on Appeal*.

02/06/2006 HTECKLU1 00000114 10623068
01 FC:1402 500.00 OP

Real Party in Interest:

This application is assigned to Infineon Technologies AG and Nokia Mobile Phones Ltd. of München, Germany and Espoo, Finland. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 22-29 and 32-34 are rejected and are under appeal. Claims 30 and 31 were cancelled in an amendment dated March 31, 2005. Claims 1-21 are withdrawn from consideration.

Status of Amendments:

No claims were amended after the final Office action. *A Notice of Appeal* was filed on November 28, 2005.

Summary of the Claimed Subject Matter:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention relates to filter devices. The present invention especially relates to acoustic wave filter devices, e.g. Surface Acoustic Wave (SAW) filter devices, Bulk Acoustic Wave (BAW) filter

devices and/or Stacked Crystal Filter (SCF) devices. Furthermore, the present invention relates to a method for fabricating filter devices.

Appellants further stated on page 16 of the specification, line 12, that, Figs. 8 to 10 show a method of fabricating filter devices according to a first embodiment of the present invention.

Appellants further explained on page 16 of the specification, line 15, that, as shown in Fig. 8, a silicon carrier wafer 50 is provided, which already contains a finalized acoustic wave filter 51. The acoustic wave filter 51 can be selected from a wide range of different acoustic wave filter types such as Surface Acoustic Wave (SAW) filters, Bulk Acoustic Wave (BAW) filters and/or Stacked Crystal Filters (SCF). Preferably, the acoustic wave filter 51 includes at least one Bulk Acoustic Wave (BAW) resonator and/or Stacked Crystal Filters (SCF) as described with respect to Figs. 1 to 7. In addition to the acoustic wave filter 51, the carrier wafer 50 includes a non-illustrated integrated circuit (IC), preferably a radio-frequency integrated circuit (RF-IC). Furthermore, the carrier wafer 50 includes pads 52 which are later used to connect the acoustic wave filter 51 to the outside world.

Appellants further explained on page 17 of the specification, line 4, that, in order to protect the acoustic wave filter 51 from contaminating or otherwise harmful external material, a silicon capping wafer 53 is provided, which will be bonded to the carrier wafer 50. In the present embodiment, the capping wafer 53 is structured to provide pad openings 54 and a recess 55, so that a cavity for the acoustic wave filter 51 is provided once the wafer bonding process is finished. A layer 56 of solder material is provided on a surface of the capping wafer 53 which confronts the carrier wafer 51.

Appellants further explained on page 18 of the specification, line 21, that, interconnections are produced following the thinning process. According to the present embodiment, a so-called "bumping process" is used to fabricate the interconnections. Bumping processes usually require some non-illustrated under-bump metallization (UBM), which has already been deposited on the pads 52 before the wafer bonding. Preferably, a structured deposition of bump materials (bump deposits) using selective deposition methods, such as microform electroplating or lift-off techniques, is performed. Thereafter the remaining under-bump metallization (UBM) is etched utilizing the bump deposits as an etch mask, and a bump formation is performed by a reflow process that melts the alloy and forms bump balls 58 which are shown in Fig. 10 as part of a resulting structure.

Appellants further stated on page 19 of the specification, line 9, that, thereafter, a wafer dicing process is performed which separates the bonded wafers into single or individual filter devices, so that each filter device includes a carrier substrate carrying at least one filter and a capping substrate. The filter is disposed in at least one cavity located between the carrier substrate and the capping substrate. The resulting filter device may then be connected to a wiring substrate using a standard flip-chip technology.

Appellants further explained on page 19 of the specification, line 25, that, the filter devices shown in Fig. 10 include a capping wafer 53 that was structured to provide pad openings 54. Fig. 12 shows a filter device according to a further embodiment of the present invention wherein a carrier substrate 60 is structured to provide openings. Accordingly, the bumping process that is used to fabricate interconnections 68 is applied to a back surface of the carrier wafer.

Appellants finally explained on page 21 of the specification, line 1, that, the carrier substrate 70 and the flip-chip-mounted substrate (die) 71 are covered by the capping wafer 74 and sealed within a cavity 76. The filter device shown in Fig. 14 may then be connected to a wiring substrate by a standard flip-chip technology using connections 78.

References Cited:

6,078,299	Funada, et al.	June 20, 2000
4,409,570	Tanski	October 11, 1983
6,720,846 B2	Iwashita, et al.	April 13, 2004
5,932,950	Yamada, et al.	August 3, 1999

Grounds of Rejection to be Reviewed on Appeal

1. Whether or not claims 22-24 and 29 are anticipated by Funada et al. (U.S. Patent No. 6,078,299) (hereinafter "Funada") under 35 U.S.C. §102.

2. Whether or not claims 25 and 26 are obvious over Funada (U.S. Patent No. 6,078,299) in view of Tanski (U.S. Patent No. 4,409,570) under 35 U.S.C. §103.

3. Whether or not claims 27 and 28 are obvious over Funada (U.S. Patent No. 6,078,299) in view of Iwashita et al. (U.S. Patent No. 6,720,846 B2) (hereinafter "Iwashita") under 35 U.S.C. §103.

4. Whether or not claims 32-34 are obvious over Funada (U.S. Patent No. 6,078,299) in view of Yamada et al. (U.S. Patent No. 5,932,950) (hereinafter "Yamada") under 35 U.S.C. § 103.

Argument:

Whether or not claim 22 is anticipated by Funada under 35 U.S.C. §102.

Claim 22 is not anticipated by Funada under 35 U.S.C. §102:

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 22 calls for, *inter alia*:

at least one interconnection for coupling the at least one filter to a wiring substrate using flip-chip technology, the interconnection being a solder or metal bump.

The Funada reference discloses a surface acoustic wave device mounted with a resin film and a method of making the same. As shown in Figs. 6A-6D of Funada, which are provided below, a piezoelectric substrate (11) has a surface wave propagation area (14), electrode pads (15) and bumps (16), and is adhered to the circuit substrate (12). Thereby, cavities (17) are created which include the surface wave propagation areas (14), and the bumps of substrate (11) are contacted to the electrode pads (15) of the substrate (12).

FIG. 6A

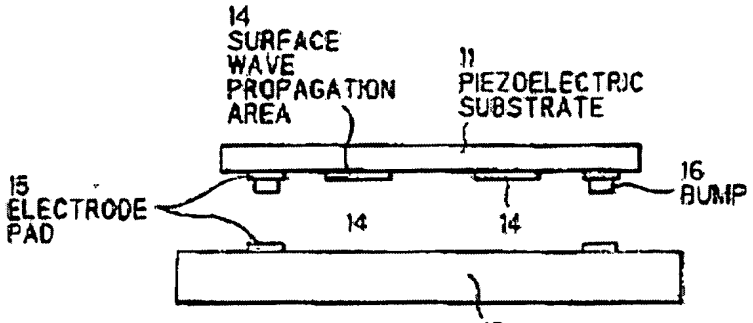


FIG. 6B

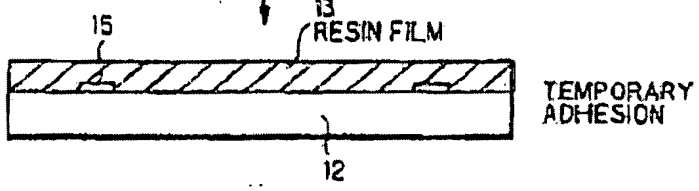


FIG. 6C

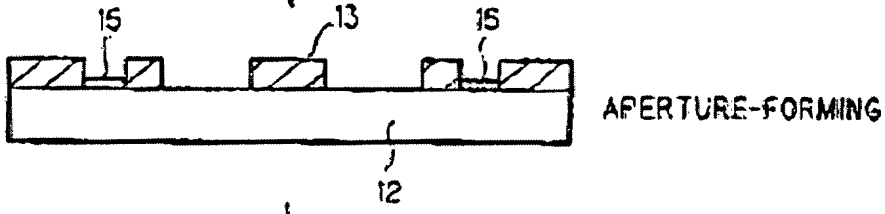
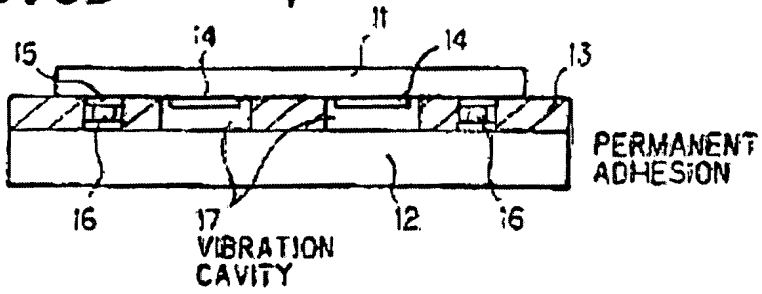


FIG. 6D



As can be seen from the above given comments, the reference does not show at least one interconnection for coupling the at least one filter to a wiring substrate using flip-chip technology, the interconnection being a solder or metal bump, as recited in claim 22 of the instant application.

Furthermore, there are many flip chip technologies known in the art. For instance, besides solder or metal bumping, stud bumping, adhesive bumping etc. may be named. However, solder or metal bumping is particularly useful in the present application for the following reasons:

1. In contrast to polymer based glue, a metal or solder seal will generate a hermetic cavity. Therefore, there will be no humidity diffusing in and out the cavities. This is an important benefit for the lasting functionality of the filter device.

2. In contrast to polymer based glue, a metal or solder seal allows electrical connections to be made between two bonded wafers.

3. Metal or solder bonding can be done at moderate temperature, i.e. at temperatures lower than 300°C. Such

temperatures are compatible with the metallization on the device and will not cause any damage to the device. This is contrary to anodic bonding, which is revealed to be not suitable for the production of the BAW, as the required temperatures and process conditions damage the filter devices.

4. Metal or solder bonding allows relatively relaxed flatness tolerances because the seal still works on wafers with a certain degree of flatness problems. In the case of other bonding techniques, such as atomic force bonding, e.g. "Si-fusion bonding", there are challenging problems in dealing with imperfect flatness. Accordingly, the present invention is not restricted to perfectly flat wafers, which provides an overall economic added value of the invention.

In summary, there are many advantages that exist when metal or solder bumping is applied. Neither metal nor solder bumping is disclosed in Funada.

In item 5 of the final Office action, the Examiner refers to Figs. 1-9 and the description in column 4, line 10 to column 8, line 10 of Funada to support her view that the interconnection is a solder or metal bump. Also, in item 12 of the final Office action, the Examiner responded to Appellant's argument that Funada does not disclose the

interconnection being a solder or metal bump by stating that "however, a person of ordinary skill in the art would recognize that Funada teaches the interconnection being a solder or metal bump (see Fig. 6A-9)." The Examiner's position **is not** supported by Funada or by the general knowledge in the art. As disclosed above, there are several techniques of bump manufacturing that are known in the art. Furthermore, the solder or metal bumps provide several advantages especially when applied in the filter device according to the instant application. Appellants cannot find any disclosure in Funada supporting the Examiner's position. Accordingly, the Examiner's position that the interconnection in Funada is a metal or solder bump is simply not correct.

Moreover, Funada discloses that the piezoelectric substrate (11) is contacted to the circuit substrate (12), which is also part of the filter, via the electrode pads (15) and the bumps (16). In the present invention as claimed, the bumps 58 are provided for connecting the entire acoustic wave filter to the outside world by using flip-chip technology (page 19, lines 15-16). This difference is very important as the filter of the present invention as claimed, can be manufactured independently from the circuit with which it is connected and then connected by a flip-chip technology step. This is contrary to Funada, where the cavity of the filter is created

with the circuit substrate itself, and where the bumps disclosed by Funada serve as a connection **within** the filter between the piezoelectric substrate (11) and the circuit substrate (12). This is contrary to the invention of the instant application as claimed, which recites at least one **interconnection** for coupling the at least one **filter to a wiring substrate** using flip-chip technology, the interconnection being a solder or metal bump.

In summary, in the present invention as claimed, the filter itself and not only the upper substrate of the filter is coupled to a wiring substrate. Even if the Examiner incorrectly considers the circuit substrate (12) of Funada to be a "coupling substrate", Funada does not anticipate the claimed feature of claim 22 of the instant application. This is because Funada discloses bumps for connecting the upper substrate with the lower substrate **and not** for **connecting** the entire **filter** with the **outside** world. As seen from the above-given remarks, the Examiner's allegations are not correct. Therefore, the Honorable Board is respectfully requested to disregard the Examiner's comments.

The Examiner's comments in item 13 on page 5 of the final Office action are not applicable. More specifically, the Examiner alleges that "if the prior art structure is capable

of performing the intended use, then it meets the claim." As seen from the above-given comments, the structure of Funada is not capable of performing the intended use. Therefore, Funada does not meet the claim. It is, therefore, respectfully submitted that the Examiner's comments pertaining to intended use be disregarded.

The Examiner's comments in item 13 on page 6 of the final Office action are not appropriate. More specifically, the Examiner stated with respect to the recitation "using flip-chip technology", that "the patentability of a product does not depend on its method of production". The phrase "using flip-chip technology" describes the structure of the interconnection between the filter and the wiring substrate. It is not used to describe a process for the manufacture of the product. Therefore, the Examiner's comments with respect to product-by-process claims are incorrect. It is, therefore, respectfully submitted that the Examiner's comments concerning product-by-process claims be disregarded.

The Examiner's comments in items 15-18 are merely statements pertaining to case law. While the statements therein may be true, it is not seen how they pertain to the present case, as Funada does not meet the structure of the present invention as claimed. Furthermore, the Examiner has not given any examples

as to how the remarks pertain to the present invention as claimed. It is, therefore, respectfully submitted that the Examiner's comments in items 15-18 should be disregarded.

Since claim 22 is believed to be allowable, dependent claims 23, 24, and 29 are believed to be allowable as well.

Claims 25 and 26 are not obvious over Funada in view of Tanski under 35 U.S.C. §103:

Since claim 22 is believed to be allowable, claims 25 and 26 are believed to be allowable as well.

Claims 27 and 28 are not obvious over Funada in view of Iwashita under 35 U.S.C. §103:

Since claim 22 is believed to be allowable, dependent claims 27 and 28 are believed to be allowable as well.

Furthermore, in item 14 on page 6 of the final Office action the Examiner contests the disqualification of the Iwashita reference as prior art. More specifically, the Examiner stated that "however, the international application PCT/EP/0100554 was filed on January 18, 2001 that is after November 2000." While it is true that January 18, 2001 is

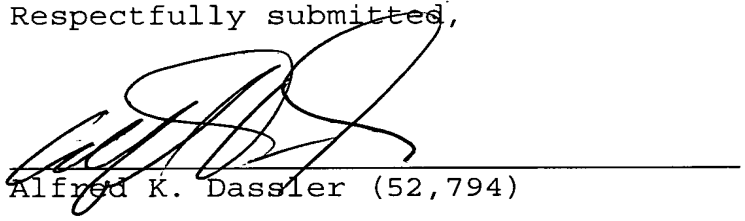
after November 2000, it is not seen how November 2000 is a relevant date. November 2000 does pertain to the availability of a PCT application to be used as **prior art**; the Iwashita reference was not a PCT application. The Iwashita reference has a U.S. filing date of March 20, 2002, which is after January 18, 2001, the effective U.S. filing date of the instant application (see 35 U.S.C. §365). Accordingly, Iwashita is unavailable as prior art. It is, therefore, respectfully submitted that the Examiner's comments in item 14 pertaining to Iwashita, be disregarded.

Claims 32-34 are not obvious over Funada in view of Yamada under 35 U.S.C. §103:

Since claim 22 is believed to be allowable, dependent claims 32-34 are believed to be allowable as well.

Based on the above-given comments, the honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,



Alfred K. Dassler (52,794)

AKD/av

Date: January 23, 2006
Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, Florida 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

Claims Appendix:

22. A filter device, comprising:

a carrier substrate;

at least one filter carried by said carrier substrate;

a capping substrate;

said carrier substrate and said capping substrate defining at least one cavity therebetween containing said at least one filter; and

at least one interconnection for coupling said at least one filter to a wiring substrate using flip-chip technology, said interconnection being a solder or metal bump.

23. The filter device according to claim 22, wherein said at least one filter is an acoustic wave filter.

24. The filter device according to claim 22, wherein said at least one filter is a Surface Acoustic Wave filter.

25. The filter device according to claim 22, wherein said at least one filter is a Bulk Acoustic Wave filter including at least one Bulk Acoustic Wave resonator.

26. The filter device according to claim 22, wherein said at least one filter is a Stacked Crystal Filter.

27. The filter device according to claim 22, wherein said carrier substrate includes an integrated circuit.

28. The filter device according to claim 27, wherein said integrated circuit is a radio-frequency integrated circuit.

29. The filter device according to claim 22, which further comprises at least one contact pad for coupling said at least one filter to a wiring substrate through at least one bonding wire.

32. The filter device according to claim 22, which further comprises passive components provided on said capping substrate.

33. The filter device according to claim 22, which further comprises additional filters disposed as flip-chips on top of said carrier substrate within said at least one cavity.

34. The filter device according to claim 33, wherein said additional filters are at least one of acoustic wave filters and active/passive ICs.

Evidence Appendix:

No evidence pursuant to && 1.130, 1.131, or 1.132 or any other evidence has been entered by the Examiner and relied upon by appellant in the appeal.

Related Proceedings Appendix:

Since there are no prior or pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal, no copies of decision rendered by a court or the Board are available.